onTAP® Series 4000 with ProScan
Boundary Scan Test Software

XILINX USB PLATFORM JTAG Cable

Installation and Setup Instructions for onTAP

onTAP Series 4000 Application Note
Flynn Systems Corporation

Installing and Using the Xilinx Platform USB Cable

This guide is designed to assist with installation of the Xilinx USB Cable. If you experience any problems or have technical questions regarding our boundary scan product, please contact our Technical Support department by email at ***support@flynn.com.*** We are happy to assist with your questions and your project. PLEASE DO NOT CONTACT XILINX REGARDING THE XILINX USB CABLE AND ITS USE WITH onTAP BOUNDARY SCAN SOFTWARE.

Please be advised, however, that support for the Xilinx USB Platform cable is limited.

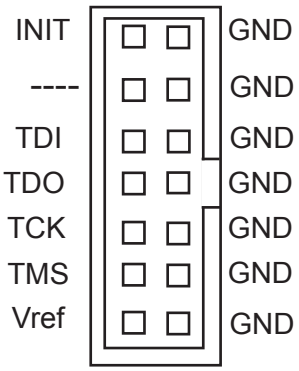
onTAP Boundary Scan Software provides limited support for the Xilinx Platform USB Cable for JTAG testing and programming. It is an ideal tool for single chain applications, and can be used to replace the Xilinx parallel port programming cables, while offering higher speeds.

The cable may be used for the following applications:

- **JTAG Test, including memory and cluster test**
- **Flash programming**
- **FPGA, CPLD and PROM configuration**
- **General purpose I/O**

Users must make sure the latest version of Xilinx ISE 9.1 or later is installed and running on their PC.

Ribbon Cable Connector & Flying Lead Pin Assignment



Pinout Assignments

Pin Name (JTAG)	Flying Lead Wire	Ribbon Cable	Description
TDI	**2**	**10**	***Test Data In*** This is the target serial input data stream for JTAG operations and is connected to the TDI Pin on the first device in the JTAG chain
TDO	**3**	**8**	***Test Data Out*** This is the target serial output data stream for JTAG operations and is connected to the TDO pin on the last device in the JTAG Chain
TCK	**5**	**6**	***Test Clock*** This is the clock signal for JTAG operations and is connected to the TCK pin on all devices that share the same data stream
TMS	**1**	**4**	***Test Mode Select*** This is the JTAG mode signal that establishes appropriate TAP state transition for the target devices which share the same data stream
INIT	**4**	**14**	***Initialize*** This pin is available for general purpose I/O such as TRST (Test Reset) control or WE (Write-Enable) for FLASH Memory
Vref	**7**	**2**	***Target Reference Voltage*** **This pin should be connected to a voltage bus on the target system that supplies the JTAG interface**
GND	**6**	**1,3,5,7, 9,11,13**	**Digital Ground All odd-numbered pins on the ribbon cable should be connected to digital ground, reducing crosstalk to a minimum**

INSTALLING THE XILINX PLATFORM USB CABLE

The Xilinx Platform USB Cable attaches to a PC with an A-to-Mini USB cable provided by Xilinx with the purchase of the Xilinx USB Platform Cable.

1. Download and run http://www.flynn.com/files/downloads/add_xilinx_usb.exe . This file will place DLLs and essential data for the Xilinx USB cable in four folders within onTAP, bin, lib, data, and msg. In addition a batch command file, onTAP with Xilinx USB.bat , is placed in the onTAP folder

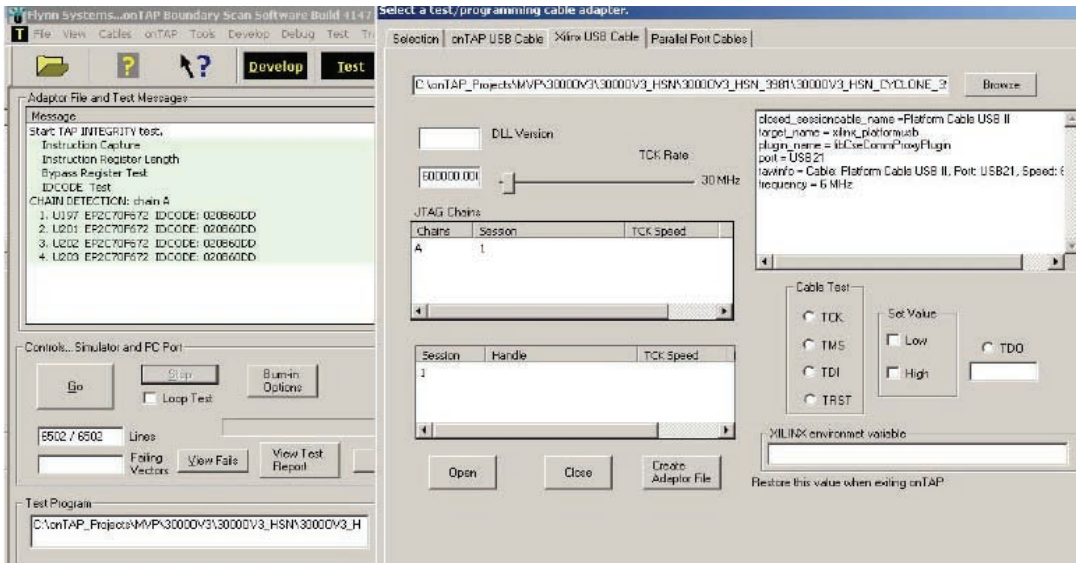
2. Delete the libCseJtag.dll file from the onTAP folder. This file is backed up in the onTAP/Xilinx_cable_no_use folder, and it should be placed in the onTAP folder when a cable other than the Xilinx cable is being used.

3. With ISE installed, run IMPACT – Configure device using Boundary Scan (JTAG) – The default is “Automatically connect to a cable and identify Boundary Scan chain.” (Once installed and configured, IMPACT does not need to be running.)

4. Run the “onTAP with Xilinx USB.bat” file to start onTAP. A shortcut can be created to access this file from the desktop.

5. From the Test screen, select Test and Programming Cable. With the Xilinx USB Cable tab selected, browse to the SVF file to be run.
   a) Select “Close” and then “Open” in the box marked “Cable.”
   b) Click “OK”.

6. From the Test screen browse to the SVF file to be run and click “GO”.



Known Problem areas include:

1. Installation procedure as described above.
2. Enumerating Xilinx cables when unplugged/plugged.
3. Managing multiple USB cables.
4. Managing the INIT pin on the cable.
5. Installation problems have been observed with Windows 7 OS and with 64 bit PCs.